METHODS AND APPARATUS FOR REDUCING THE SIZE OF CODE WITH AN EXPOSED PIPELINE BY ENCODING NOP OPERATIONS AS INSTRUCTION OPERANDS

ABSTRACT OF THE DISCLOSURE

A method for reducing total code size in a processor having an exposed pipeline may include the steps of determining a latency between a load instruction, and a using instruction and inserting a NOP field into the defining or using instruction. When inserted into the load instruction, the NOP field defines the following latency following the load instruction. When inserted into the using instruction, the NOP field defines the latency preceding the using instruction. In addition, a method for reducing total code size during branching may include the steps of determining a latency following a branch instruction for initiating a branch from a first point to a second point in an instruction stream, and inserting a NOP field into the branch instruction. Further, a method according to this invention may include the steps of locating delayed effect instructions followed by NOPs, such as load or branch instructions, within a code; deleting the NOPs from the code; and inserting a NOP field into the delayed effect instructions. Apparatus according to this invention may include a processor including a code containing a delayed effect instruction, wherein the delayed effect instruction includes a NOP field.